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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/826,805	04/16/2004	Shih-Chang Shei	JCLA12240	1474

7590 07/12/2006

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 07/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/826,805	SHEI ET AL.	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-23 and 27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-23 and 27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 12-23 and 27 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification recites chip 210 connected to circuits of circuit board 226 via the first patterned conductive film and the second patterned conductive film. Since the circuits are integrated on the circuit board, then, even if none of the circuits on the circuit board includes a chip, chip 210 is also integrated on the circuit board. Therefore, there is no support for chips connected to the first patterned conductive film and the second patterned conductive film, wherein no integrated circuit (IC) chip is connected to the first patterned conductive film and the second patterned conductive film, as recited in claim 12.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 12, 14-20, 23 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murata (6,483,184) in view of Durocher et al. (6,614,103).

Regarding claim 12, Murata teaches in figure 1 and related text a chip package structure, comprising:

a submount 18 having a first surface and a second surface opposite to the first surface, a plurality of grooves 18a on sidewalls of the submount;

a first patterned conductive film on a first part of the first surface 20, a first part of the second surface 26 and on a part of an inner wall of the grooves 28;

a second patterned conductive film on a second part of the first surface 20, a second part of the second surface 26 and a remaining part of the inner wall of the grooves 28; and

a chip 14 on the mount, wherein the chip has two electrodes (connected to 34) electrically connecting with the first and second patterned conductive reflection films 20, respectively.

Murata does not teach using the package for a flip-chip light emitting diode chip, such that no integrated circuit (IC) chip is connected to the first patterned conductive film and

the second patterned conductive film, wherein the chip is formed inside an indentation of the submount.

Durocher et al. teach in figure 12 using a package for a flip-chip light emitting diode chip 59, wherein the light emitting diode chip 59 is formed inside an indentation of the submount.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a flip-chip light emitting diode chip in Murata's package and to be formed inside an indentation of the submount, in order to use the device in an application which requires a flip-chip light emitting diode chips, and in order to improve the characteristics of the device and to provide better protection to the chip, respectively.

Note that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

Note that by using the package for a flip-chip light emitting diode chip, no integrated circuit (IC) chip will be connected to the first patterned conductive film and the second patterned conductive film.

Note that in prior art's device the first and second patterned conductive reflection films will be disposed on the sidewalls and bottom of the indention, because the first and second patterned conductive reflection films must be connected to the chip.

Regarding claims 3-9, 14-20, 23 and 27, prior art teaches m is a number of the grooves that are on a first sidewall of the submount and n is a number of the grooves that are on a second sidewall of the submount,

wherein the first sidewall and the second sidewall are adjacent to each other,

wherein the first sidewall and the second sidewall are opposite to each other,

wherein m is equal and not equal to n,

wherein m and n are 1 and greater than 1,

wherein the grooves are on disposed on a sidewall at a corner of the submount, and

wherein an angle formed between the sidewall and the bottom of the indentation is an obtuse angle.

Regarding claims 10 and 21, prior art does not teach using bumps comprise Sn-Pb alloy, Sn-Au alloy or Au. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use bumps comprise Sn-Pb alloy, Sn-Au alloy or Au in prior art's device in order to improve the contact resistance of the device with known materials in the art.

Claims 13 and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murata and Durocher et al., as applied to claim 12 above, and further in view of Applicant Admitted Prior Art (AAPA).

Regarding claim 13 and 21, Murata and Durocher et al. teach substantially the entire claimed structure, as applied to claim 12 above, except two bumps disposed between the electrodes of the LED chip and the first patterned conductive film and the second patterned conductive film. AAPA teaches in figure 1B two bumps 106 disposed between the electrodes of the LED chip and the first patterned conductive film and the second patterned conductive film. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use two bumps disposed between the electrodes of the LED chip and the first patterned conductive film and the second patterned conductive film in prior art's device in order to reduce the contact resistance between the chip and the conductive films.

Regarding claim 22, Murata and Durocher et al. do not teach a submount comprises a material selected from the group consisting of aluminum nitride, boron nitride and zinc oxide. AAPA teaches a submount comprises a material selected from the group consisting of aluminum nitride, boron nitride and zinc oxide. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a submount comprises a material selected from the group consisting of aluminum nitride, boron nitride and zinc oxide in prior art's device in order to improve the contact resistance of the device with known materials in the art.

Response to Arguments

Applicant argues that layer 57 of Durocher is just for reflection and is not a part of the electrode layer.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., first and second patterned conductive reflection films being part of the electrode layers) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
7/4/06

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